ABSTRACT OF THE DISCLOSURE

A method for forming within a substrate employed within a microelectronics fabrication a damascene multi-layer conductor interconnection layer with inhibited/attenuated damage to a conductor stud layer accessed therein within a trench, when forming the trench interconnection pattern within a dielectric layer overlying the conductor stud layer. There is provided a substrate having a contact region formed therein employing a first intermediate metal dielectric (IMD) layer having a pattern of via contact holes etched through the IMD layer filled with studs of conductor material. There is then planarized the surface of the IMD contact region. There is then formed over the planarized first IMD layer contact region a blanket composite etch stop layer. There is the formed over the blanket composite etch stop layer a second blanket inter-level metal dielectric (IMD) layer. A patterned photoresist etch mask layer formed into the interconnection trench pattern is then formed over the substrate and employed to transfer the trench pattern into the second IMD layer and the upper sub-layer of the composite etch stop layer. The interconnection trench pattern is then transferred by a second subtractive etch into the lower sub-layer of the composite etch stop layer, employing the second IMD layer as an etch mask A barrier metal layer is then formed over the substrate. The trench pattern is then filled with a second conductor material to complete the damascene multi-layer conductor interconnection layer, with improved electrical conductivity and contact properties and inhibited/attenuated degradation effects due to processing on the damascene interconnection layer.